FIG. 1 (Related Art)

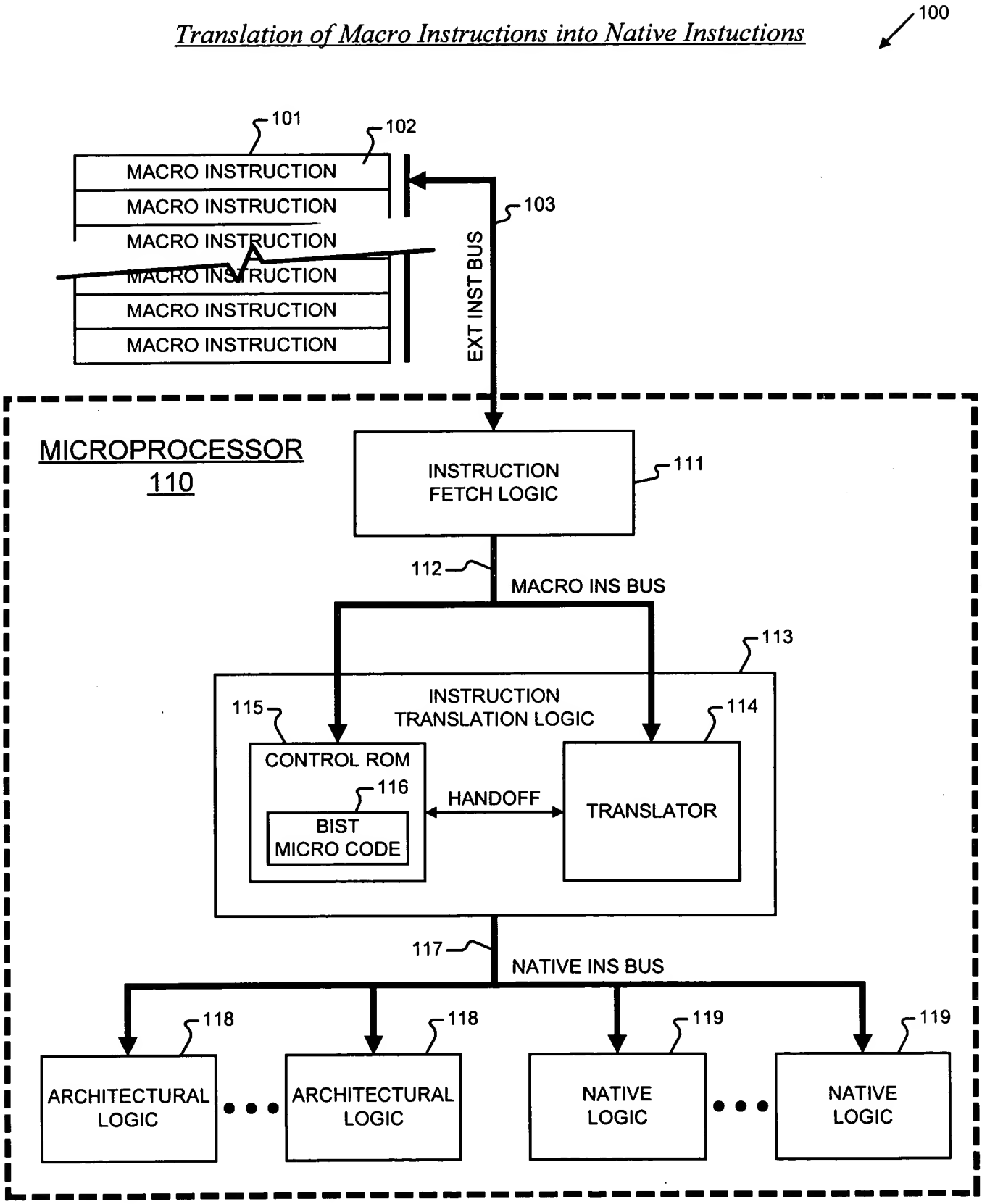

FIG. 2 (Related Art)

Indirect Specification of Native Register via Macro Instruction

200

Cycle	Macro Ins Bus	Native Ins Bus
1	ADD [EAX],FFFFFFFFh	***
2	***	LD NR1,[EAX]
3	***	ADD NR1,NR1,FFFFFFFFh
4	***	ST [EAX],NR1

3 CYCLES

FIG. 3

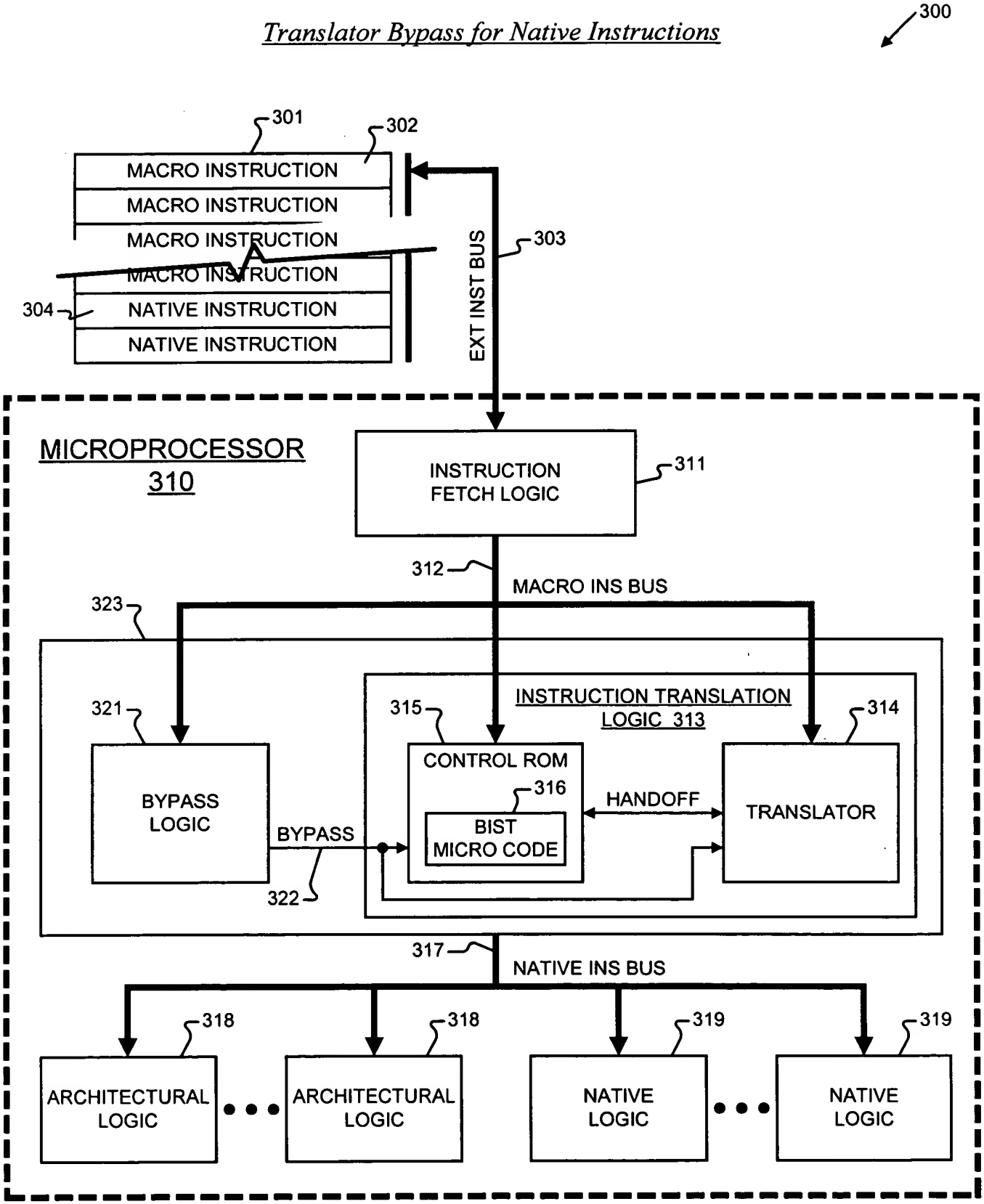
Translator Bypass for Native Instructions
300
301
302
MACRO INSTRUCTION
MACRO INSTRUCTION
MACRO INSTRUCTION
MACRO INSTRUCTION
304
NATIVE INSTRUCTION
NATIVE INSTRUCTION
EXT INST BUS
303
MICROPROCESSOR
310
INSTRUCTION
FETCH LOGIC
311
312
MACRO INS BUS
323
321
315
INSTRUCTION TRANSLATION
LOGIC 313
314
CONTROL ROM
316
BYPASS
LOGIC
BYPASS
BIST
MICRO CODE
HANDOFF
TRANSLATOR
322
317
NATIVE INS BUS
318
318
319
319
ARCHITECTURAL
LOGIC
ARCHITECTURAL
LOGIC
NATIVE
LOGIC
NATIVE
LOGIC

FIG. 4

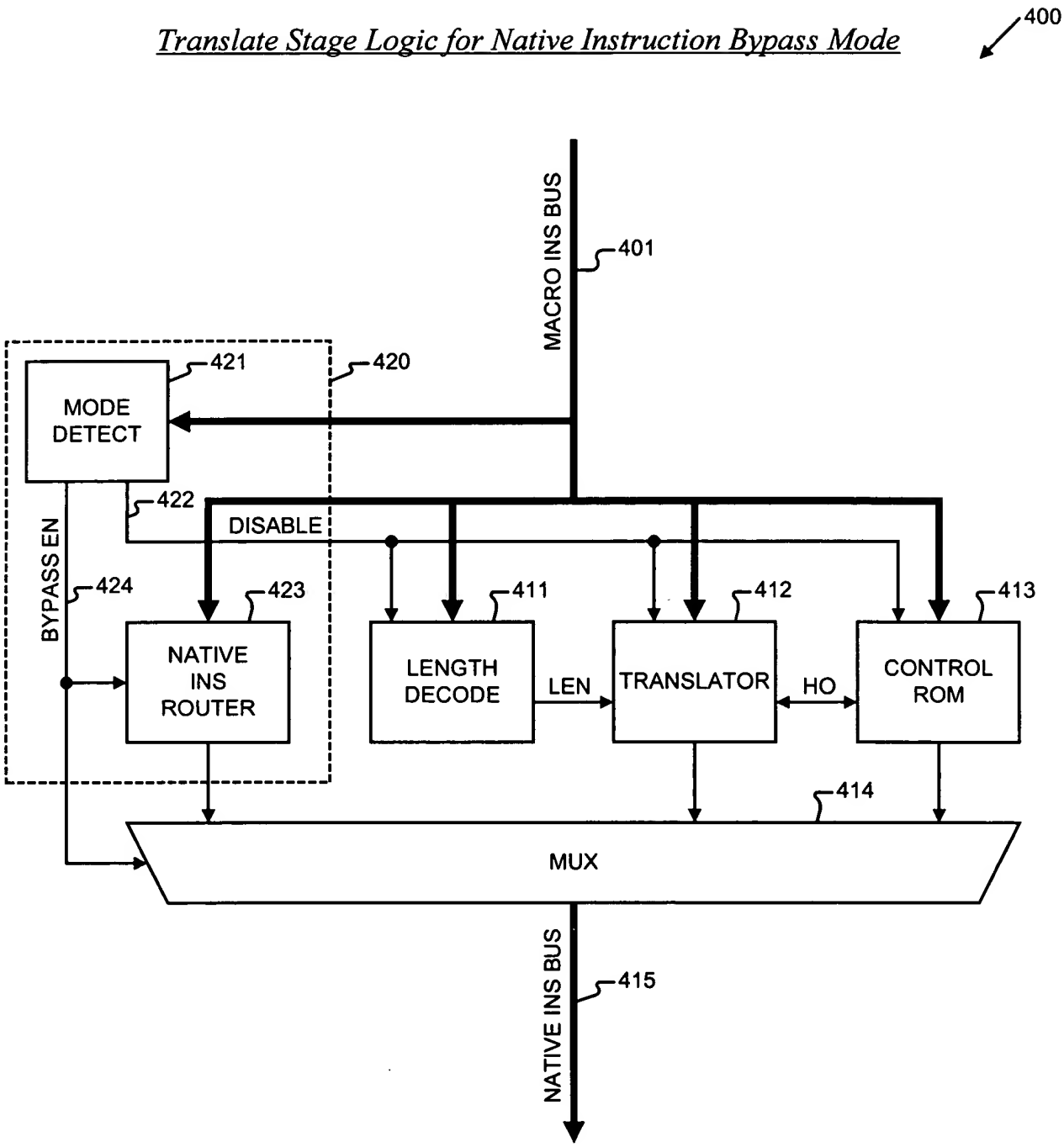
Translate Stage Logic for Native Instruction Bypass Mode
400
MACRO INS BUS
401
MODE DETECT
421
420
422
DISABLE
BYPASS EN
424
423
411
412
413
NATIVE INS ROUTER
LENGTH DECODE
LEN
TRANSLATOR
HO
CONTROL ROM
414
MUX
NATIVE INS BUS
415

FIG. 5

Using Microcode to Test Native Resources

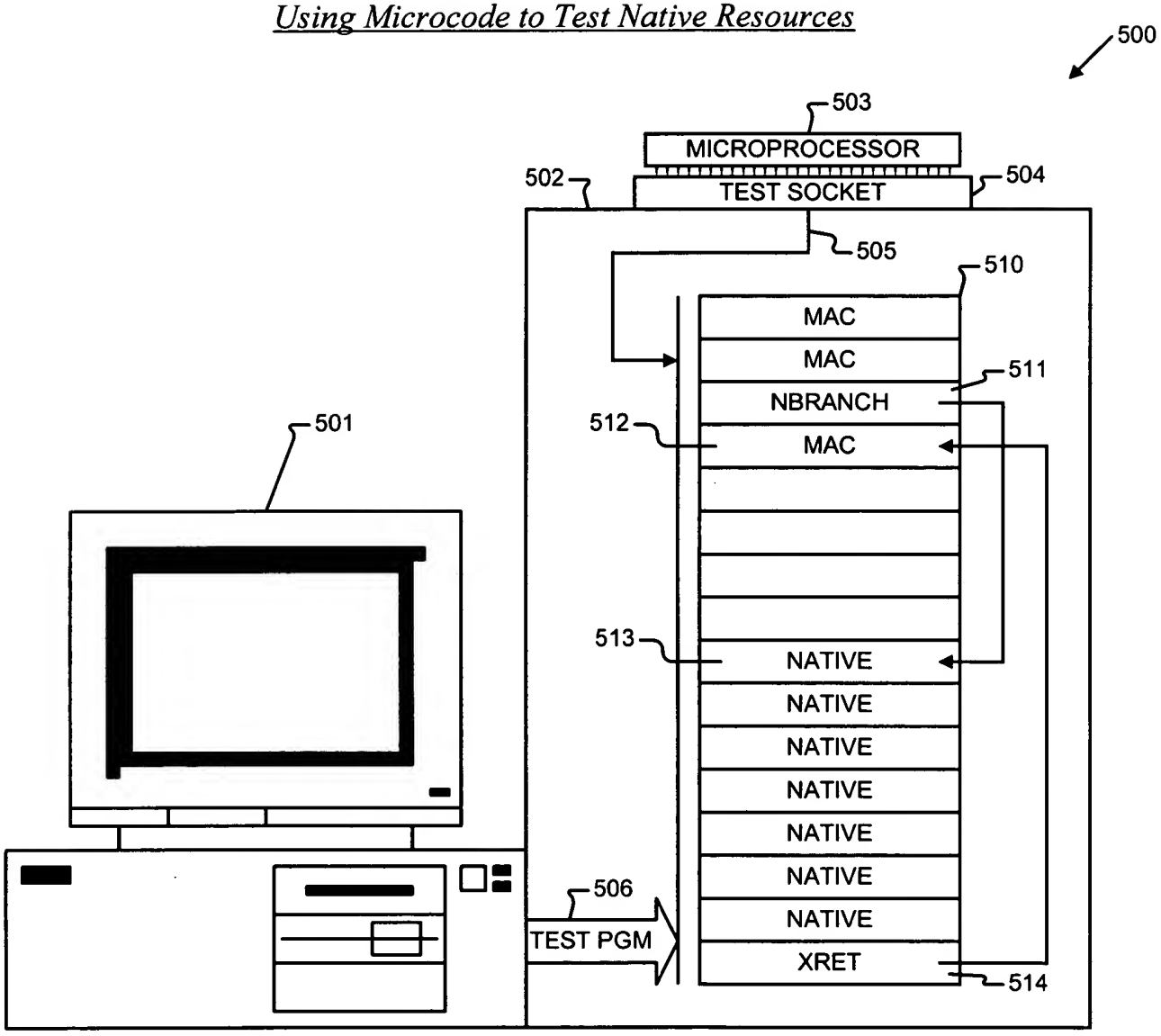

FIG. 6

Instruction Sequence for Testing Native Registers

600

Cycle	Macro Ins Bus	Native Ins Bus
1	MOV EAX,*TST1*	+++
2	MOV EBX,*OUTBFR*	LD EAX,*TST1*
3	NBRANCH	LD EBX,*OUTBFR*
4	LD T1,0	JMP [EAX]
5	ST [EBX],T1	LD T1,0
6	NOT T1	ST [EBX],T1
7	ST [EBX],T1	NOT T1
8	+++	ST [EBX],T1
9	+++	+++
10	+++	+++
1001	XRET	+++
1002	NEXT MAC	JMP [EAX+1]
1003	***	NEXT MAC